IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each semiconductor substrate element of said substrate elements including integrated circuitry, comprising:

providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side in a first wafer having a periphery having a portion thereof including a flat;

providing a second semiconductor substrate element having a first side including integrated circuitry thereon and having a backside in a second wafer having a periphery having a portion thereof including a flat;

providing a heat sink element for said multi-level stack of semiconductor substrate elements;

stacking said first semiconductor substrate element and the second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the second semiconductor substrate element having the periphery of said first semiconductor substrate element substantially aligned with the periphery of said second semiconductor substrate element, said first semiconductor substrate element and the second semiconductor substrate element for locating a portion of the integrated circuitry on said first semiconductor substrate element vertically spaced from a portion of the integrated circuitry on the second semiconductor substrate element for vertical alignment of said first semiconductor element and said second semiconductor substrate element; and

severing from said stack traversely at least one dice pair comprising a die from said first semiconductor substrate element and a second die from said second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said second semiconductor substrate element.

2. (Original) The method of claim 1, wherein said adhesive comprises a dielectric adhesive.

3. (Currently Amended) The method of claim 1, further including:
disposing the [a] heat sink element between said first semiconductor substrate element and said second semiconductor substrate element.

4. (Previously Presented) The method of claim 1, wherein said first semiconductor substrate element and the second semiconductor substrate element, each semiconductor substrate element of the first semiconductor element and the second semiconductor element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Canceled)

6. (Previously Presented) The method of claim 1, further comprising:
connecting a first die of said at least one dice pair to a substrate having conductors.

7. (Original) The method of claim 6, wherein said connection is selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. (Previously Presented) The method of claim 6, further comprising:
connecting both dice of said at least one dice pair to said conductors of said substrate.

9. (Original) The method of claim 6, further comprising:
connecting the second die of said at least one dice pair to portions of the conductors of said substrate through intermediate connection elements.

10. (Previously Presented) The method of claim 9, wherein said intermediate connection elements are selected from a group consisting of bond wires and traces of flex circuits.

11. (Previously Presented) The method of claim 10, further comprising:

connecting said at least one dice pair to portions of the conductors of said substrate and encapsulating said at least one dice pair thereafter.

12. (Withdrawn) A method of fabricating a multi-level stack of semiconductor wafer segments, each of said semiconductor wafer segments including integrated circuitry, comprising:

providing a first semiconductor substrate segment having a first side including integrated circuitry thereon and having a back side;

providing at least one second semiconductor substrate segment having a first side including a plurality of integrated circuits thereon and having a backside;

stacking said first semiconductor substrate segment and said at least one second semiconductor substrate segment in at least partially superimposed relationship to form a stack of semiconductor wafer segments;

separating said stack to form at least two semiconductor wafer segment stacks, each said semiconductor wafer segment stack comprising a first semiconductor wafer segment having a side including integrated circuitry and a back side and at least one second semiconductor wafer segment having a side including integrated circuitry and a back side,

stacking said at least two semiconductor wafer segment stacks in at least partially superimposed relationship;

locating bond pads on said first semiconductor wafer segment of at least one of said at least two semiconductor wafer segment stacks on a side adjacent said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack at a periphery thereof;

forming a notch through said at least one second semiconductor wafer segment of said at least one semiconductor wafer segment stack, said notch extending between and substantially perpendicular to a circuitry side and a back side of said at least one second semiconductor wafer segment to provide access to at least one said peripheral bond pad of said first semiconductor wafer segment of said at least one semiconductor wafer segment stack; and

adhesively attaching said first and said at least one second semiconductor wafer segments of said at least one semiconductor wafer segment stack.

13. (Withdrawn) The method of claim 12, further including:

stacking said semiconductor wafer segments of said at least one semiconductor wafer segment stack with the integrated circuitry side of said first semiconductor wafer segment proximate the back side of said at least one second semiconductor wafer segment; and

locating said bond pads on said integrated circuitry side of said first semiconductor wafer segment.

14. (Withdrawn) The method of claim 12, further including:

adhesively attaching said first and said at least one second semiconductor wafer segments of said at least one semiconductor wafer segment stack.

15. (Withdrawn) The method of claim 12, further including

disposing a heat sink element between said first and said at least one second semiconductor wafer segments.

16. (Withdrawn) The method of claim 12, further comprising:

connecting at least one of said first and said at least one second semiconductor wafer segment to conductors of a substrate.

17. (Withdrawn) The method of claim 16, wherein said connection comprises a connection element selected from a group comprising bond wires and traces of flex circuits.

18. (Withdrawn) A method of fabricating a multi-level stack of semiconductor wafers, each of said semiconductor wafers including integrated circuitry, comprising:

providing a first semiconductor wafer having a first side including integrated circuitry and having a back side;

providing at least one other semiconductor wafer having a first side including integrated circuitry and having a back side;

stacking said first semiconductor wafer and said at least one other semiconductor wafer in a superimposed relationship;

locating bond pads on said first semiconductor wafer of said stack on a side proximate said at least one other semiconductor wafer at a periphery thereof;

forming a notch through said at least one other semiconductor wafer, said notch substantially perpendicular to a circuitry side and the back side of said at least one other semiconductor wafer providing access to at least one said peripheral bond pads of said first semiconductor wafer of said stack; and

adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer.

19. (Withdrawn) The method of claim 18, further including:

stacking said first semiconductor wafer and said at least one other semiconductor wafer with a third semiconductor wafer, having the integrated circuitry side of said first semiconductor wafer segment proximate said back side of said third semiconductor wafer.

20. (Withdrawn) The method of claim 18, wherein said adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer comprises:

adhesively attaching said first semiconductor wafer and said at least one other semiconductor wafer with a dielectric adhesive.

21. (Withdrawn) The method of claim 18, further including:

disposing a heat sink element between said first semiconductor wafer and said at least one other semiconductor wafer.

22. (Withdrawn) The method of claim 18, further comprising:

connecting at least one of said first semiconductor wafer and said at least one other semiconductor wafer to conductors of a substrate.

23. (Withdrawn) The method of claim 22, wherein a direct electrical connection is achieved with a connection element selected from a group comprising bond wires and traces of flex circuits.

24. (Withdrawn) The method of claim 18, wherein said first semiconductor wafer and said at least one other semiconductor wafer are stacked with the integrated circuit side of said first semiconductor wafer facing the back side of said at least one other semiconductor wafer, and wherein said bond pads are located on the integrated circuit side of said first semiconductor wafer.